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Michael Schlansker, Nagabhushan Chitlur, Erwin Oertli, Paul M. Stillwell, Jr, Linda Rankin, Dennis Bradford, Richard J. Carter, Jayaram Mudigonda, Nathan Binkert, Norman P. Jouppi
November 2007 SC '07: Proceedings of the 2007 ACM/IEEE conference on Supercomputing
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Data centers and HPC clusters often incorporate specialized networking fabrics to satisfy system requirements. However, Ethernet's low cost and high performance are causing a shift from specialized fabrics toward standard Ethernet. Although Ethernet's ...

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2 [FaCSim: a fast and cycle-accurate architecture simulator for embedded systems](#)



Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, Kwangsub Kim, SangYong Han
June 2008 ACM SIGPLAN Notices, Volume 43 Issue 7
Publisher: ACM

 Full text available: [Pdf](#) (664.75 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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There have been strong demands for a fast and cycle-accurate virtual platforms in the embedded systems area where developers can do meaningful software development including performance debugging in the context of the entire platform. In this paper, ...

Keyw ords: architecture simulator, cycle-accurate simulation, full-system simulation, simulator parallelization, virtual prototyping

3 [Proactive fault tolerance for HPC with Xen virtualization](#)



Arun Babu Nagarajan, Frank Mueller, Christian Engelmann, Stephen L. Scott
June 2007 ICS '07: Proceedings of the 21st annual international conference on Supercomputing
Publisher: ACM

 Full text available: [Pdf](#) (526.85 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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Large-scale parallel computing is relying increasingly on clusters with thousands of processors. At such large counts of compute nodes, faults are becoming common place. Current techniques to tolerate faults focus on reactive schemes to recover from ...

Keyw ords: high-performance computing, proactive fault tolerance, virtualization

4 [Implementing the scale vector-thread processor](#)



Ronny Krashinsky, Christopher Batten, Krste Asanović

July 2008 ACM Transactions on Design Automation of Electronic Systems (TODAES),
Volume 13 Issue 3

Publisher: ACM

Full text available: [Pdf](#) (11.74 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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The Scale vector-thread processor is a complexity-effective solution for embedded computing which flexibly supports both vector and highly multithreaded processing. The 7.1-million transistor chip has 16 decoupled execution clusters, vector load and ...

Keyw ords: Vector processors, hybrid C++/Verilog simulation, iterative VLSI design flow, multithreaded processors, procedural datapath pre-placement, vector-thread processors

5 [FaCSim: a fast and cycle-accurate architecture simulator for embedded systems](#)



Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, Kwangsub Kim, SangYong Han

June 2008 LCTES '08: Proceedings of the 2008 ACM SIGPLAN-SIGBED conference on
Languages, compilers, and tools for embedded systems

Publisher: ACM

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